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(54) Error correction system in a multicarrier radio transmission system.

(57) This invention relates to a multicarrier radio transmission system with error correction means. Several carriers are modulated by parallel data signals respectively. Each data signal is added frame alignment bits simultaneously. At receiving end, while frame alignment of data signal, transmitted on one carrier, is not established, error correction of the data signal is done based on frame alignment of other data signal transmitted on other carrier.

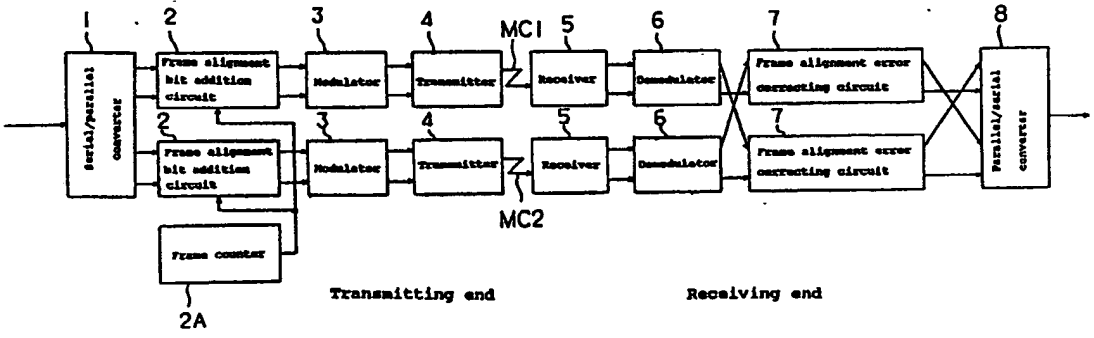

Figure 1 Block diagram showing one embodiment of the present invention

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Error correction system in a multicarrier radio transmission system

Background of the Invention

Field of the Invention

This invention relates to a multicarrier radio transmission system and, in particular, to an error correcting method in the radio transmission system.

Recent radio transmission systems with their increasing transmission capacities tend to use multilevel or multi-carrier schemes. They also require forward error correction to improve the system gain. Some synchronization is needed for such error correction. In particular, synchronism must be held where the error rate is as high as about 10^{-2}.

Description of the Prior Art

Figure 2 is a block diagram of a conventional scheme. In this figure, component 1 is a serial/parallel converter; component 2 is a frame alignment bit addition circuit; component 2A is a frame counter; component 3 is a modulator; component 4 is a transmitter. These circuits are provided at the transmitting end. Frame alignment bit addition circuit 2, frame counter 2A, modulator 3, and transmitter 4 are provided in two sets.

For example, when a 100 Mb/s signal is fed to serial/parallel converter 1, it is branched to four 25 Mb/s signals. Each combination of two 25 Mb/s signals is fed to frame alignment bit addition circuit 2, where a frame alignment bit is added. The position of frame alignment bit addition is controlled by frame counter 2A provided for each frame alignment bit addition circuit 2.

The signal from each frame alignment bit addition circuit 2 is fed to modulator 3 to achieve 4PSK for example, then is transmitted on a carrier depending on transmitter 4. In this example, one 100 Mb/s signal is radio transmitted on two separate carriers.

Component 5 is a receiver; component 6 is a demodulator; component 7 is a frame alignment error correcting circuit; component 8 is a parallel/serial converter. These circuits are provided at the receiving end. Receiver 5, demodulator 6, and frame alignment error correcting circuit 7 are provided in two sets corresponding to as many carriers.

The signal on each carrier enters receiver 5, is demodulated by demodulator 6, and is fed to frame alignment error correcting circuit 7, where frame alignment is established. Error correction is performed according to the established alignment position.

The signal from each frame alignment error correcting circuit 7 is fed to parallel/serial converter 8, which converts the four 25 Mb/s signals into a 100 Mb/s signal.

The above conventional scheme, however, involves the following problem. Among two radio transmission circuits MC1 and MC2, if circuit MC2 is considerably deteriorated, frame alignment is lost at frame alignment error correcting circuit 7 corresponding to circuit MC2. As a result, error correction becomes impossible on the MC2 signal. This causes the error rate of the 100 Mb/s output to be 1/4, thus lowering the system gain.

Summary of the Invention

This invention is aimed to provide an error correction method for multicarrier radio transmission systems in order to solve the above problem involved in the conventional scheme. If one of multiple radio transmission circuits is considerably deteriorated, the method allows error correction to be performed by keeping frame alignment for the signal on the deteriorated circuit.

This error correction method for multicarrier radio transmission systems is characterized by its frame alignment detection code addition circuits which are configured so that they are controlled by a common frame counter and its frame alignment error correcting circuits which are configured so that they are supplied with different carrier signals.

In this configuration, each frame alignment detection code addition circuit at the transmitting end adds a code for frame alignment detection to the signal; the frame alignment detection code addition circuits are controlled by a common frame counter so that they insert codes for frame alignment detection at an identical position.

At the receiving end, different carrier signals are fed to the frame alignment error correcting circuits.

Even if some of the multiple radio transmission circuits are considerably deteriorated, frame alignment can be established using the carrier signal from a transmission circuit which is not deteriorated because the frame alignment error correcting circuits are supplied with different carrier signals. This permits the deteriorated transmission circuit to keep frame alignment and allows errors to be corrected on that transmission circuit.

Brief Description of the Drawings

Figure 1 is a block diagram showing one embodiment of this invention.

Figure 2 is a block diagram showing a conventional scheme.

Description of the Preferred Embodiment of the Invention

An embodiment of this invention is described below with reference to a drawing.

Figure 1 is a block diagram showing an embodiment of this invention. In Figure 1, the transmitting end is provided with serial/parallel converter 1, frame alignment bit addition circuit 2, frame counter 2A, modulator 3, and transmitter 4. Two sets of frame alignment bit addition circuit 2, modulator 3, and transmitter 4 are provided. Frame counter 2A serves two frame alignment bit addition circuits 2. As a result, the positions of frame alignment bit insertion are identical on both signals.

The receiving end is provided with receiver 5, demodulator 6, frame alignment error correcting circuit 7, and parallel/serial converter 8. Receiver 5, demodulator 6, and frame alignment error correcting circuit 7 are provided in two sets corresponding to as many carriers.

Frame alignment error correcting circuits 7 are designed so that they are supplied with different carrier signals. If one of radio transmission circuits MC1 and MC2 is considerably deteriorated, frame alignment error correcting circuits 7 are still supplied with different carrier signals.

At the transmitting end in the above configuration, serial/parallel converter 1 branches a 100 Mb/s signal (for example) into four 25 Mb/s signals. The combination of two 25 Mb/s signals is fed to frame alignment bit addition circuit 2, where a frame alignment bit is added to each of the two signals. Frame alignment bit addition circuits 2 are controlled by common frame counter 2A so that the frame alignment bit is inserted at an identical position on both signals.

The signal from each frame alignment bit addition circuit 2 is fed to modulator 3 to achieve 4PSK for example, then is transmitted on a carrier depending on transmitter 4. In this example, one 100 Mb/s signal is radio transmitted on two carriers.

At the receiving end, the signal on each carrier is fed to receiver 5, is demodulated by demodulator 6, and is fed to frame alignment error correcting circuit 7, which establishes frame alignment and corrects errors according to the established alignment position.

The signal from each frame alignment error correcting circuit 7 is fed to parallel/serial converter 8, which converts the four 25 Mb/s signals into one 100 Mb/s signal.

Suppose that one – MC1 for example – of multiple radio transmission circuits MC1 and MC2 is considerably deteriorated. Since frame alignment error correcting circuits are still supplied with different carrier signals, frame alignment can be established using the intact carrier signal although a half of the input data is deteriorated. Therefore, the deteriorated transmission circuit MC1 can still keep frame alignment. Error correction is thus possible on the signal from the deteriorated transmission circuit. This helps increase the system gain.

In the stage of error correction, frame alignment is established according to the position of frame alignment bit insertion; however, it is also possible to detect frame alignment according to another appropriate code. For the latter scheme, frame alignment detection code addition circuits are provided to add a code for frame alignment detection in place of the frame alignment bit addition circuits. As in the case of the above embodiment, these frame alignment detection code addition circuits are controlled by a common frame counter.

It is to be understood that the foregoing description is merely illustrative of the preferred embodiments of the present invention, but that the present invention is not to be limited thereto, but is to be determined by the scope of the appended claim.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. An error correction system in a multicarrier radio transmission system, comprising;

(a) first means (1) for providing a plurality of parallel data signals;

(b) second means (2), operatively connected to said first means, for adding frame alignment bits and error correction bits to the data signals respectively and outputting framed data signals;

(c) third means (2A), operatively connected to said second means, for controlling the position of the frame alignment bits commonly to the data signals;

(d) fourth means (3), operatively connected to said second means, for modulating a plurality of carriers, which have different frequencies from each other, by the framed data signals respectively, and outputting modulated signals;

(e) fifth means (4), operatively connected to the fourth means, for transmitting the modulated signals;

(f) sixth means (5), operatively connected to the fifth means, for receiving the transmitted sig-

nals;

g) sevens means (6), operatively connected to the sixth means, for demodulating the received signals and outputting demodulated data signals;

(h) eighth means (7), operatively connected to the seventh means, for establishing frame alignment and correcting errors in the demodulated signals using the error correction bits respectively, wherein, while frame alignment of one of the demodulated data signals is not established, error corection of the one of the data demodulated signals is done based on frame alignment of other demodulated data signal.

2. An error correction system as set forth in claim 1, wherein said third means (2A) is a frame counter, which indicates timing for adding frame alignment bits.

3. An error correction system as set forth in claim 1, wherein each of said parallel data signals consist of a plurality of bits.

4. An error correction system as set forth in claim 3, wherein said first means (1) is a serial-to-parallel converter, which inputs serial signals and outputs m x n bits parallel signals.

5. An error correction system as set forth in claim 4, wherein said second means (2) consists of m frame alignment bit addition circuits, each of which inputs n bits parallel signals.

6. An error correction system as set forth in claim 5, wherein said n bits parallel signal is a two bits parallel signal.

7. An error correction system as set forth in claim 6, wherein said fourth means (3) consists of first and second 4-phase phase shift keying modulators.

8. An error correction system as set forth in claim 7, wherein said seventh means (6) consists of first and second 4-phase phase shift keying demodulators, each of which outputs two bits signals.

9. An error correction system as set forth in claim 8, wherein said eighth means (7) consists of first frame alignment error correction circuits, which inputs one bit of two bits signals ouput from the first demodulator and one bit of two bits signals output from the second demodulator, and second frame alignment error correction circuits, which inputs the other bit of two bits signals output from the first demodulator and the other bit of two bits signals output from the second demodulator.

10. An error correction system as set forth in claim 9, further comprising a parallel to serial converter (8), which inputs parallel signals output from said first and second frame alignment error correction circuits, and which outputs serial signals.

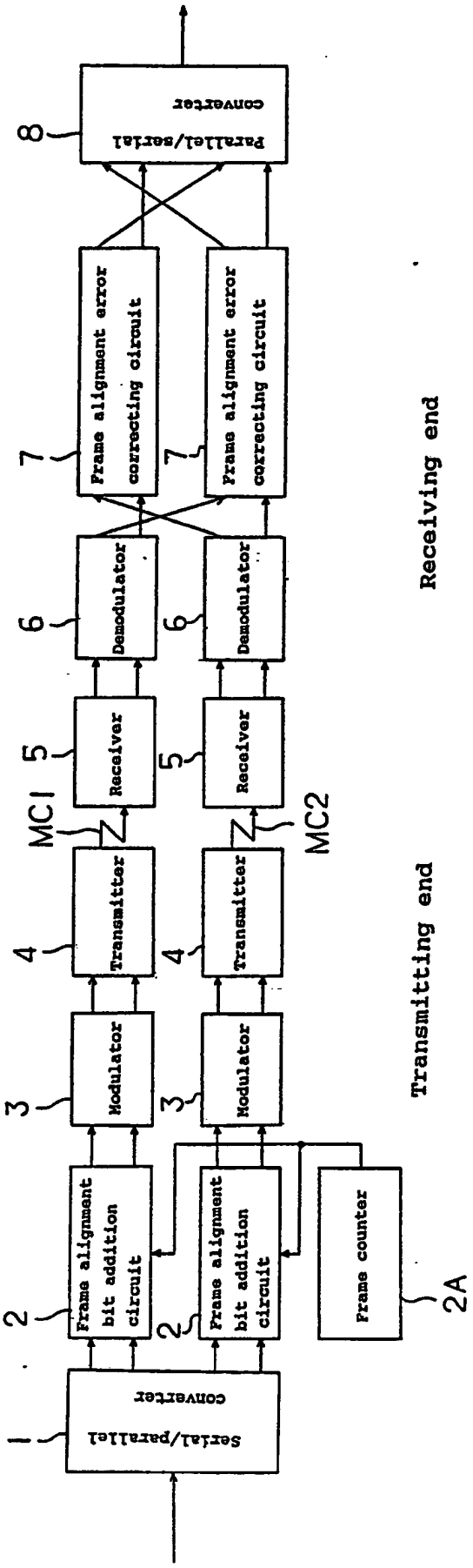

Figure 1 Block diagram showing one embodiment of the present invention

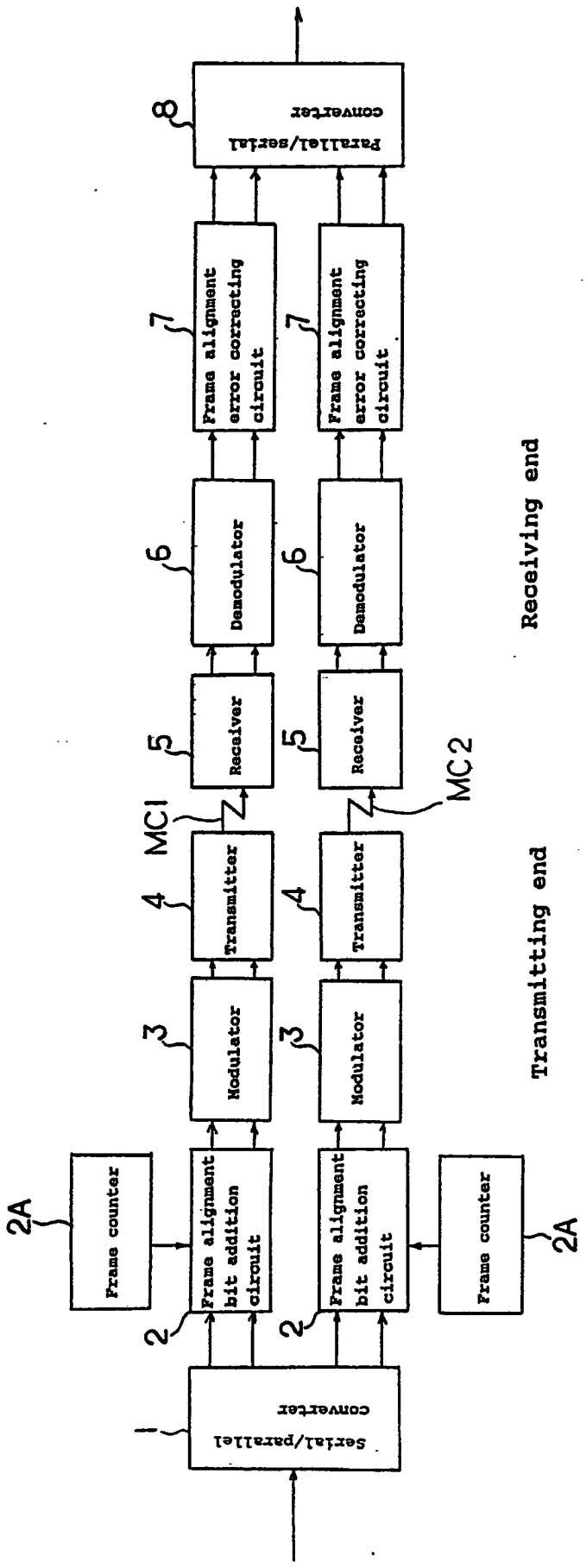

Figure 2 Block diagram showing a conventional scheme